HIP0061

60V, 3.5A, 3-Transistor Common Source ESD Protected Power MOSFET Array

December 1997

Features

- **Three 3.5A Power MOS N-Channel Transistors**
- **Output Voltage to 60V**
- **$r_{DS(ON)}$ . . . . . 0.225Ω Max Per Transistor at V_{GS} = 10V**
- **Pulsed Current . . . . . .10A Each Transistor**
- **Avalanche Energy . . . . . 100mJ Each Transistor**
- **Grounded Tab Eliminates Heat Sink Isolation**

Applications

- **Automotive**
- **Appliance**
- **Industrial Control**
- **Robotics**
- **Relay, Solenoid, Lamp Drivers**

Ordering Information

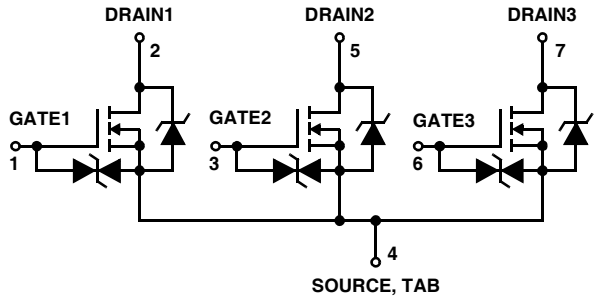
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HIP0061AS1	-40 to 125	7 Ld Staggered Vertical SIP	Z7.05C
HIP0061AS2	-40 to 125	7 Ld Gullwing SIP	Z7.05B

Description

The HIP0061 is a power MOSFET array that consists of three matched N-Channel enhancement mode MOS transistors connected in a common source configuration. The advanced Intersil PASIC2 process technology used in this product utilizes efficient geometries that provides outstanding device performance and ruggedness.

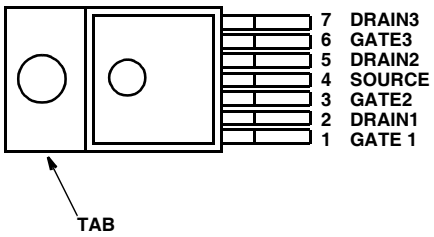
The HIP0061 is designed to integrate three power devices in one chip thus providing board layout area and heat sink savings for applications such as Motor Controls, Lamps, Solenoids and Resistive Loads.

Symbol



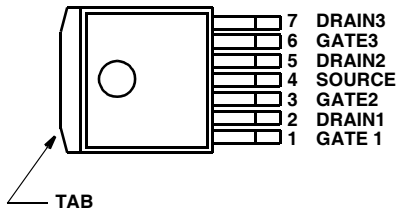
Pinouts

HIP0061AS1
(SIP - VERTICAL)
TOP VIEW



TAB (SOURCE) INTERNALLY CONNECTED TO PIN 4

HIP0061AS2
(SIP - GULLWING)
TOP VIEW



TAB (SOURCE) INTERNALLY CONNECTED TO PIN 4

Absolute Maximum Ratings $T_A = 25^oC$

Drain to Source Voltage, V_{DS}
(Over Operating Junction and Case Temperature Range) 60V
Drain to Gate Voltage, V_{DGR} 60V
Gate to Source Voltage, V_{GS} . . . . . -15, +20V
Pulsed Drain Current, I_{DM}, Each Output,
All Outputs on at V_{GS} = 10V (Notes 1, 2) 10A
Continuous Source to Drain Diode Current, I_{SD}
at V_{GS} = 10V (Note 2) 3.5A
Continuous Drain Current, I_{DS}, Each Output,
All Outputs on at V_{GS} = 10V (Note 2) 3.5A
Single Pulse Avalanche Energy, E_{AS} (Note 3) 100mJ

Operating Conditions

Temperature Range . . . . . -40^oC to 125^oC
Drain to Source On-State Voltage Range . . . . . 5V to 10V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SIP-Vertical Package	55	3
SIP-Gullwing Package	55	3

Maximum Junction Temperature, T_J . . . . . 150^oC
Maximum Storage Temperature Range, T_{STG} . . . . -55^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Back Side Potential . . . . . V- (Source, Tab)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Pulse width limited by maximum junction temperature.
2. Drain current limited by package construction.
3. V_{DD} = 25V, Start $T_J = 25^oC$, L = 15mH, $R_{GS} = 50\Omega$, I_{PEAK} = 3.5A. See Figures 1, 2, 12, and 13.
4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 100μA, V_{GS} = 0V	$T_C = -40^oC$ to 125^oC	60	-	-	V
			$T_C = 25^oC$	-	70	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA		1.8	2.3	2.7	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	$T_C = 25^oC$	-	-	1	μA
			$T_C = 125^oC$	-	-	10	μA
Forward Gate Current, Drain Short Circuited to Source	I_{GSSF}	V_{DS} = 0V, V_{GS} = 20V		-	-	100	nA
Reverse Gate Current, Drain Short Circuited to Source	I_{GSSR}	V_{DS} = 0V, V_{GS} = -15V		-	-	-100	nA
Drain to Source On Resistance (Note 5)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.5A	$T_C = 25^oC$	-	0.215	0.265	Ω
		V_{GS} = 10V, I_D = 3.5A	$T_C = 125^oC$	-	0.365	0.425	Ω
		V_{GS} = 5V, I_D = 2A	$T_C = 25^oC$	-	0.275	0.320	Ω
		V_{GS} = 5V, I_D = 2A	$T_C = 125^oC$	-	0.465	0.5	Ω
Drain to Source On Resistance Matching	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.5A	$T_C = 25^oC$	-	95	-	%
Forward Transconductance (Note 5)	g_{fs}	V_{DS} = 10V, I_D = 1A		-	2.5	-	S
Turn-On Delay Time (Note 6)	$t_{d(ON)}$	V_{DD} = 30V, $R_L = 15\Omega$, V_{GS} = +10V, I_D = 2A, $R_G = 50\Omega$ See Figure 14		-	10	-	ns
Rise Time (Note 6)	t_r			-	25	-	ns
Turn-Off Delay Time (Note 6)	$t_{d(OFF)}$			-	18	-	ns
Fall Time (Note 6)	t_f			-	12	-	ns
Total Gate Charge (Note 6)	$Q_{g(TOT)}$	V_{DS} = 50V, V_{GS} = 10V, I_D = 2A See Figures 16, 17		-	8.0	9.5	nC
Gate-Source Charge (Note 6)	Q_{gs}			-	0.7	1.0	nC
Gate-Drain Charge (Note 6)	Q_{gd}			-	3.5	4.0	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Short-Circuit Input Capacitance, Common Source	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V f = 1MHz	-	142	-	pF
Short-Circuit Output Capacitance, Common Source	C_{OSS}		-	107	-	pF
Short-Circuit Reverse Transfer Capacitance, Common Source	C_{RSS}		-	24	-	pF

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage (Note 5)	V_{SD}	I_{SD} = 2A, V_{GS} = 0V	-	0.9	1.1	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/μs	-	50	-	ns

NOTES:

5. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
6. Independent of operating temperature.

Typical Performance Curves

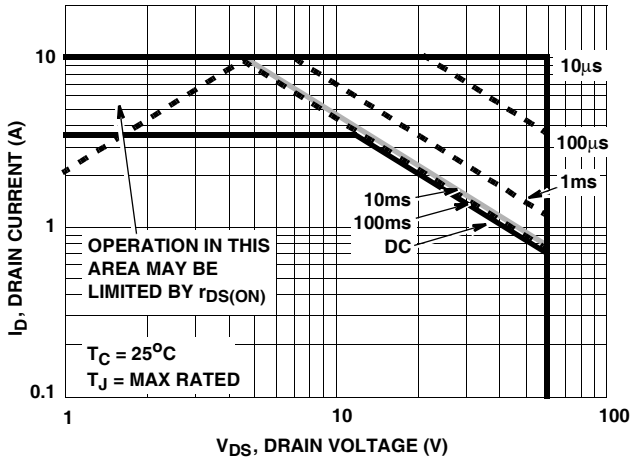


FIGURE 1A. 25°C SAFE-OPERATING AREA CURVE

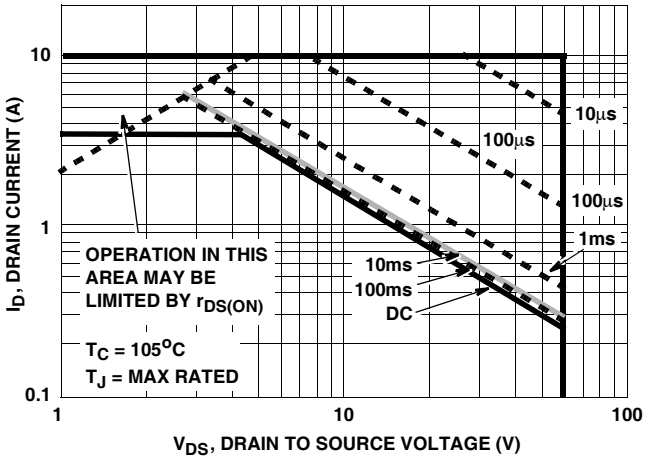


FIGURE 1B. 105°C SAFE-OPERATING AREA CURVE

Typical Performance Curves (Continued)

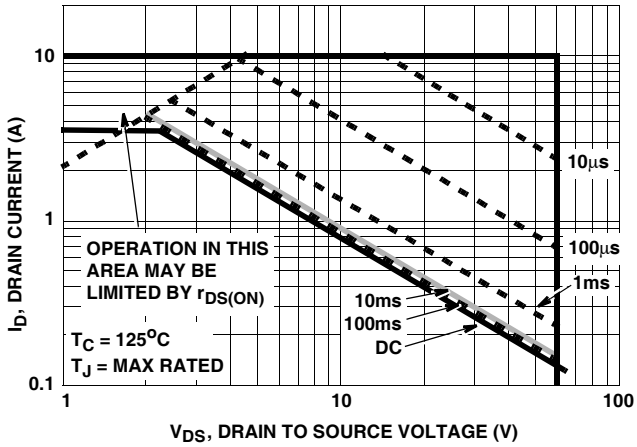


FIGURE 1C. 125°C SAFE-OPERATING AREA CURVE

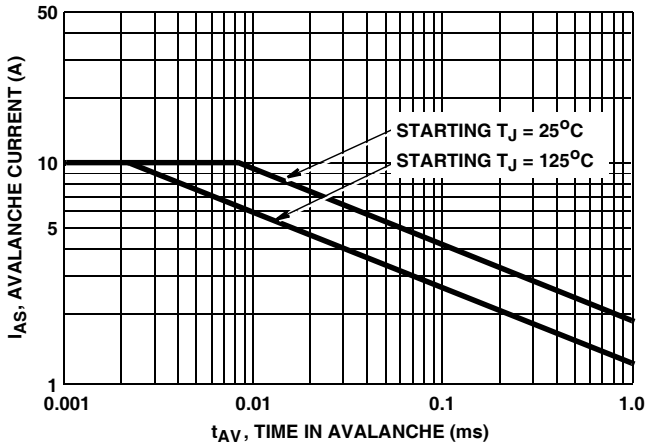


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

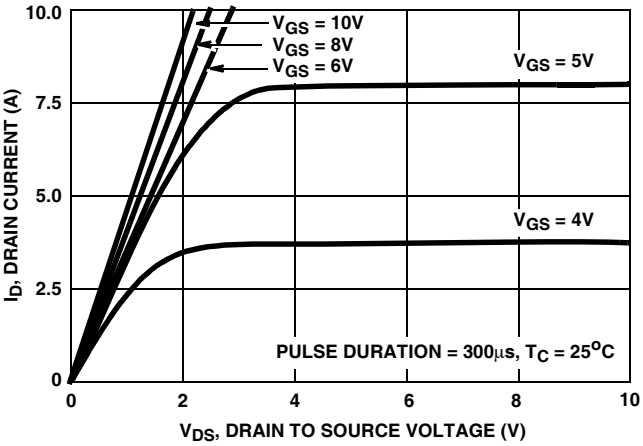


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

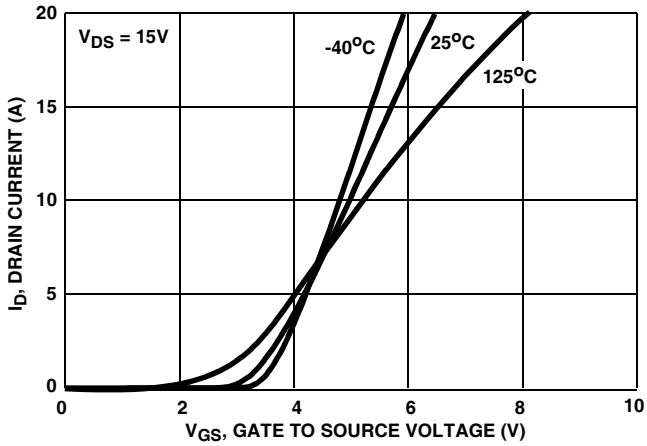


FIGURE 4. TYPICAL TRANSFER CHARACTERISTICS

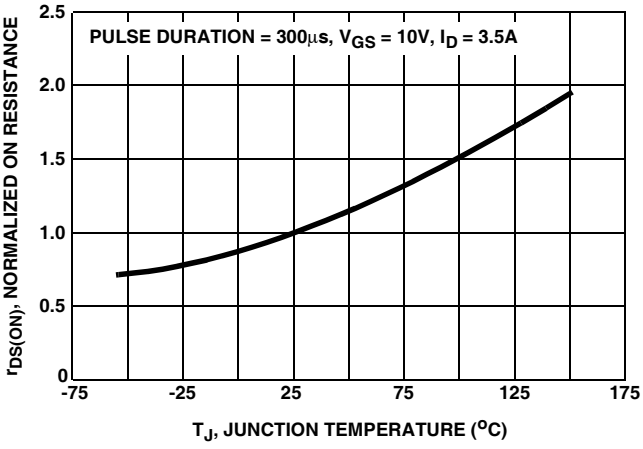


FIGURE 5. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

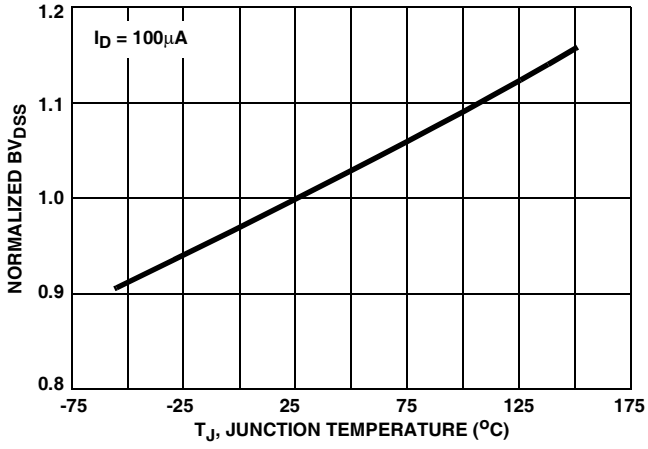


FIGURE 6. NORMALIZED BV_{DSS} vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

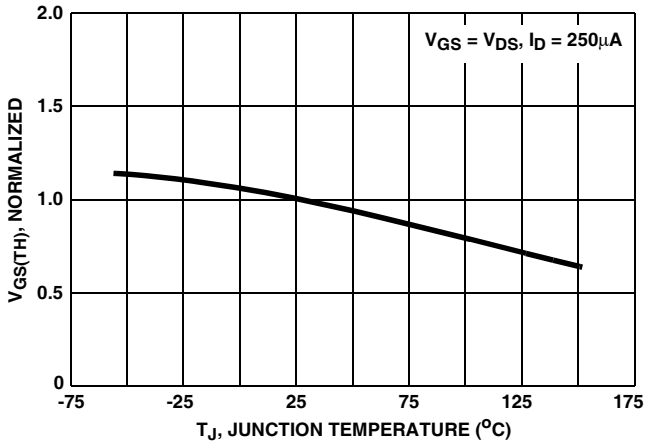


FIGURE 7. NORMALIZED $V_{GS(TH)}$ vs JUNCTION TEMPERATURE

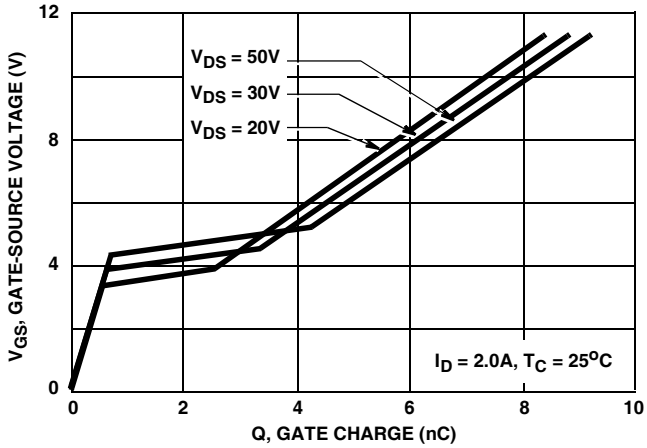


FIGURE 8. GATE-SOURCE VOLTAGE vs GATE CHARGE

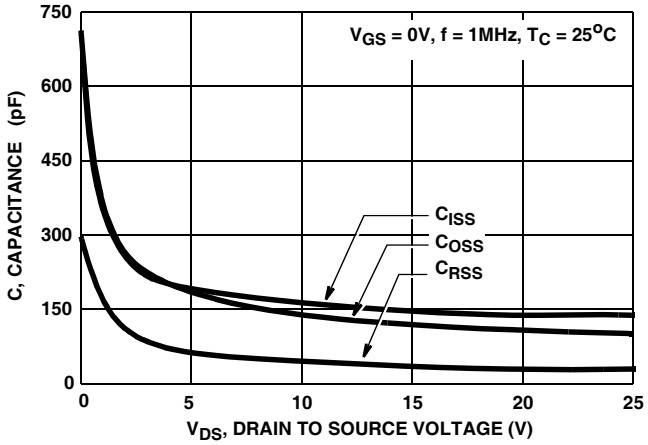


FIGURE 9. TYPICAL CAPACITANCE vs VOLTAGE

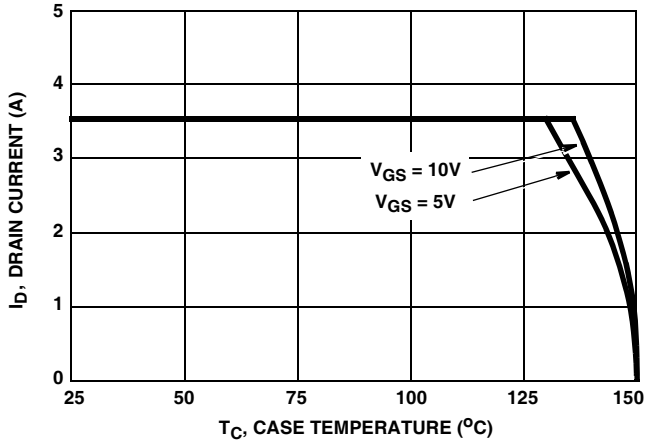


FIGURE 10. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves (Continued)

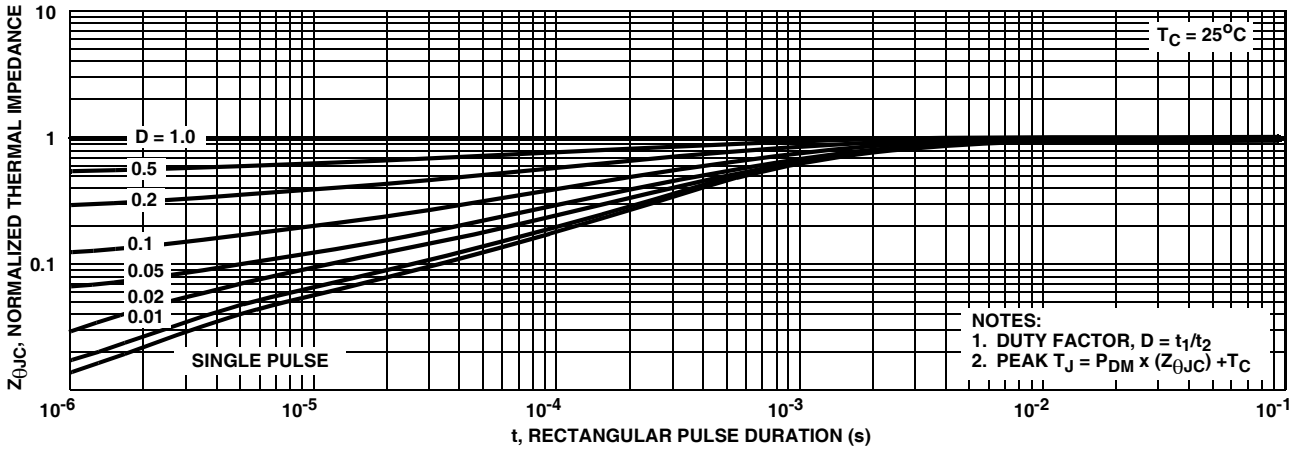


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

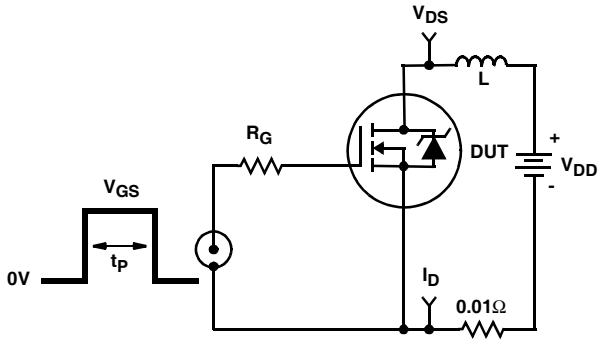


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

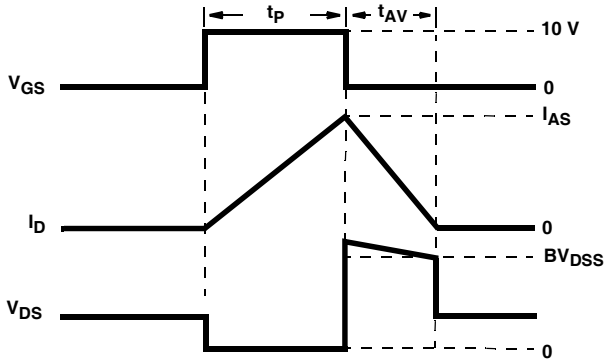


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms

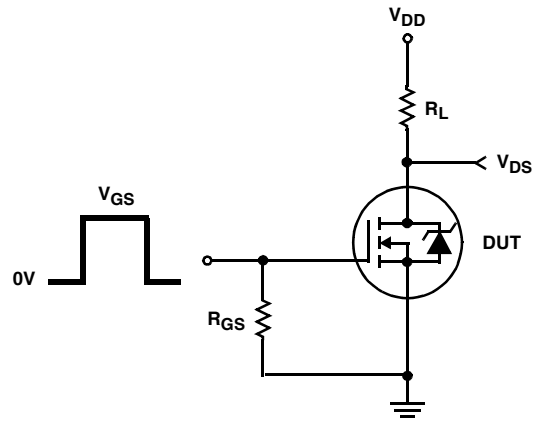


FIGURE 14. RESISTIVE SWITCHING TEST CIRCUIT

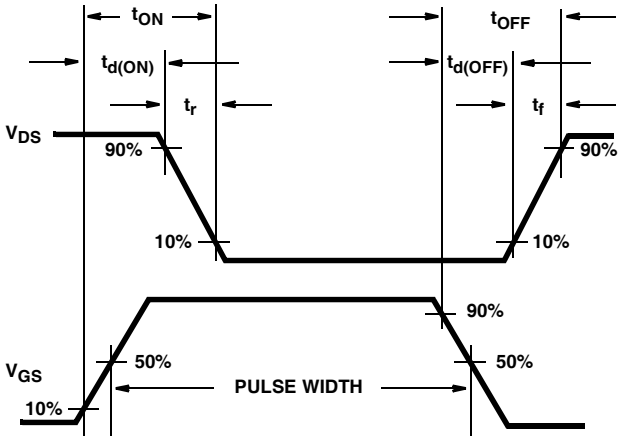


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

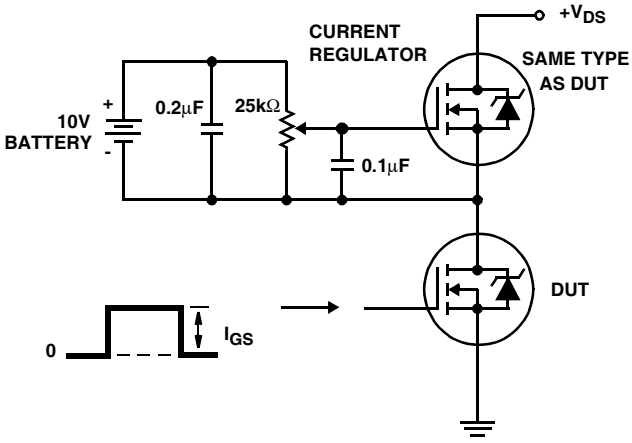


FIGURE 16. GATE CHARGE TEST CIRCUIT

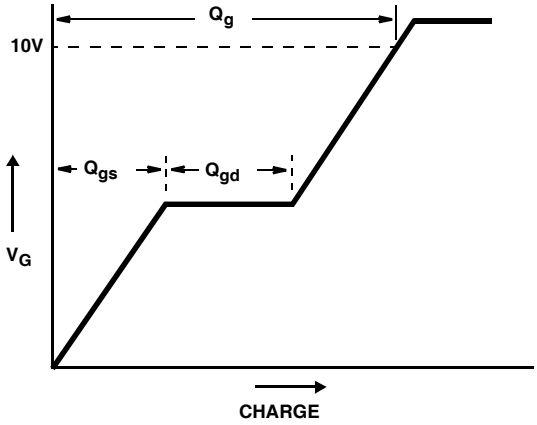


FIGURE 17. BASIC GATE CHARGE WAVEFORM

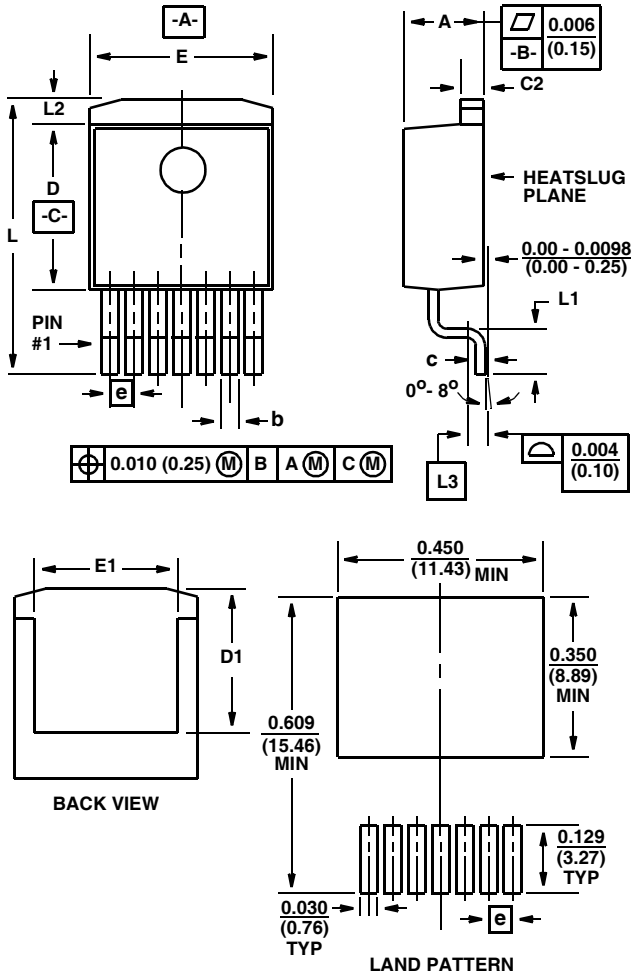
PSPICE Model Listing
Device Model Netlist for the HIP0061 Power MOSFET Array

```
*Rev: 6/12/95
.SUBCKT HIP0061 1 2 3 4 5 6 7
X1  8 1 11 4 HIP0061_1
LS1 2 8 7.5n
X2  9 3 11 4 HIP0061_1
LS2 5 9 7.5n
X3 10 6 11 4 HIP0061_1
LS3 7 10 7.5n
LS4 4 11 7.5n
.ENDS

.SUBCKT HIP0061_1   3   2   11   9
MOS1      4    2    1   1   NMOS1
JFET      13   1    4   J1
D1        5    6    D1
DBODY     1    13   D2
DBREAK    3    7    D3
DSUB      9    13   D4
DESD1     2    12   D5
DESD2     15   12   D5
VBREAK    7    1    DC 90
C21       2    1    750P
C23       2    13   45P
C24       2    4    1100P
RDRAIN    13   14   9.0e-02
LDRAIN    14   3    7.5n
RSOURCE   1    15   17.5e-03
LSOURCE   15   11   7.5n
FDSCHRG   4    2    VMEAS 1.0
E41       5    15   4   1   1.0
VPINCH    6    8    DC 10.0
VMEAS     8    15   DC 0.0
.MODEL NMOS1 NMOS LEVEL=3 (VTO=2.75 TOX=5e-08
KP=3.150e-03 PHI=0.65 GAMMA=2.55
+ VMAX=6.42e+07 NSUB=4.33e+16 THETA=0.60973
ETA=0.0015 KAPPA=1.275
+ L=1u W=3050u)
.MODEL J1 NJF (VTO=-15.0 BETA=10.736
LAMBDA=1.15e-02 PB=0.5848 IS=+1.0e-13
+ RD=3.53e-02 ALPHA=0.2)
.MODEL D1 D (IS=1.0e-15 N=0.03 RS=1.0)
.MODEL D2 D (IS=3.0e-13 RS=2.5e-03 TT=20N
CJO=350e-12)
.MODEL D3 D (IS=1.0e-13 N=1.0 RS=2.0)
.MODEL D4 D (IS=1.0e-13 RS=2.0e-03 CJO=80e-12)
.MODEL D5 D (IS=1.0e-15 RS=1.0e-03 CJO=2.5e-12)
.ENDS
```

NOTE: For further discussion of the PSPICE PowerFET macromodel consult **Spicing-Up SPICE II Software for Power MOSFET Modeling**, Intersil Application Note AN8610.

Single-In-Line Plastic Packages (SIP)



Z7.05B

7 LEAD PLASTIC SINGLE-IN-LINE PACKAGE SURFACE MOUNT "GULLWING" LEAD FORM

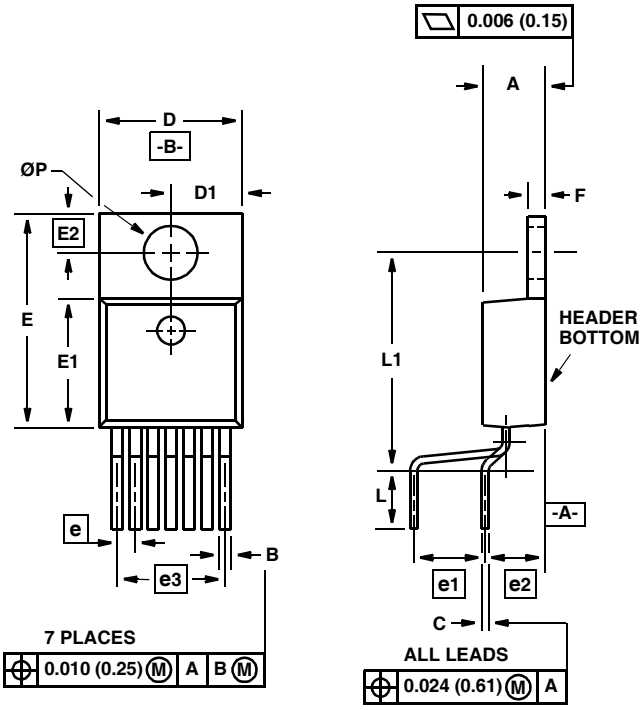
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
C2	0.048	0.055	1.22	1.39	5
D	0.350	0.370	8.89	9.39	-
E	0.395	0.405	10.04	10.28	-
D1	0.310	-	7.88	-	-
E1	0.310	-	7.88	-	-
L	0.549	0.569	13.95	14.45	-
L1	0.068	0.088	1.72	2.24	-
L2	0.045	0.055	1.15	1.40	-
L3	0.030 BSC		0.76 BSC		4
b	0.028	0.034	0.71	0.86	5, 6, 7
c	0.018	0.024	0.46	0.60	5
e	0.050 BSC		1.27 BSC		-

Rev. 2 12/95

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-169AC, Issue A.
2. Controlling dimension: Inch.
3. Dimensioning and tolerance per ANSI Y14.5M-1982.
4. Gauge plane L3 is parallel to heatslug plane.
5. Dimensions include lead finish.
6. Leads are not allowed above the datum -B-.
7. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" by more than 0.003'' (0.08mm).

Single-In-Line Plastic Packages (SIP)



Z7.05C

7 LEAD PLASTIC SINGLE-IN-LINE PACKAGE
STAGGERED VERTICAL LEAD FORM

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
B	0.028	0.034	0.71	0.86	3, 4
C	0.018	0.024	0.46	0.60	3
D	0.395	0.405	10.04	10.28	-
D1	0.198	0.202	5.03	5.13	-
E	0.595	0.605	15.11	15.37	-
E1	0.350	0.370	8.89	9.39	-
E2	0.110 BSC		2.79 BSC		
e	0.050 BSC		1.27 BSC		-
e1	0.200 BSC		5.08 BSC		-
e2	0.169 BSC		4.29 BSC		-
e3	0.300 BSC		7.62 BSC		-
F	0.048	0.055	1.22	1.39	3
L	0.150	0.176	3.81	4.47	-
L1	0.600	0.620	15.24	15.74	-
ØP	0.147	0.152	3.73	3.86	3

Rev. 0 6/95

NOTES:

1. Controlling dimension: INCH.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions include lead finish.
4. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall not cause lead width to exceed maximum “B” by more than 0.003 inches (0.08mm).

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